

ABSTRACT OF THE DISCLOSURE

A variable resolution analog-to-digital converter includes a sample-and-hold circuit including a plurality of sample-and-hold units which are connected in parallel and selectively activated corresponding to a required resolution to sample and hold an analog input signal, a plurality of conversion stages connected in cascade to an output of the sample-and-hold circuit to convert an output signal of the sample-and-hold circuit to a plurality of bit signals, and a synthesis circuit to synthesize the bit signals, to generate a digital output signal.

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